

DALLIN DAHL

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RESEARCH INTERESTS: Graph neural networks and graph-theoretic algorithms applied to hardware security and reliability — hardware IP protection, netlist reverse engineering, and trojan detection in FPGA and ASIC netlists. Exploring type systems to enhance reliability of hardware description languages.

EDUCATION

Brigham Young University

PhD, Electrical & Computer Engineering Expected Dec 2026
Dissertation: Labeling IP Cores in Unlabeled FPGA Netlists
Advisor: Dr. Jeff Goeders
BS, Computer Engineering Apr 2022
Minor: Math, Computer Science

PUBLICATIONS

D. Dahl and J. Goeders, “IPLens: GNNs for Fine-grained IP Core Identification” (in preparation)

D. Dahl, K. Faulkner, J. Usevitch and J. Goeders, “Neurocore: Characterizing the Performance of GNNs for Configurable IP Core Identification in FPGA Netlists,” ACM Transactions on Reconfigurable Technology and Systems (under review)

D. Dahl, R. McKendrick and J. Goeders, “RandSoC: Generating Large, Diverse Synthetic FPGA Benchmark Suites for ML Tooling Research”, 2026 IEEE International Conference on Field Programmable Technology (ICFPT), Honolulu, HI, USA, 2026 (to appear).

D. Dahl, K. Faulkner, J. Usevitch and J. Goeders, “Neurocore: A GNN Approach to Configurable IP Core Identification in FPGA Netlists,” 2025 IEEE International Conference on Field Programmable Technology (ICFPT), Shanghai, China, 2025, pp. 137–145, doi: 10.1109/ICFPT67023.2025.00026.

D. Dahl, C. Simpson, K. Faulkner, B. Nelson and J. Goeders, “IPRec and Isoblaze: Fuzzy Subcircuit Isomorphism for IP Detection in Physical Netlists,” 2023 IEEE Physical Assurance and Inspection of Electronics (PAINE), Huntsville, AL, USA, 2023, pp. 1–7, doi: 10.1109/PAINE58317.2023.10318012.

TEACHING EXPERIENCE

Teaching Assistant Winter 2026
Embedded Linux Systems (ECEn 427)
Duties: lab tutor, grading, writing grading infrastructure, enhancing exams.
Enrollment: ~40

Teaching Assistant Fall 2025
Embedded Systems (ECEn 330)
Duties: lab tutor, grading.
Enrollment: ~120

Instructor Spring 2025
Computer Systems (ECEn 224)
Duties: office hours, grading, writing lectures, lecturing, writing exams.
Enrollment: ~20

Undergraduate research mentor

Spring 2023–Winter 2025

Outcomes: onboarding, training, coauthor on papers (K. Faulkner)

Teaching Assistant

Fall 2020

Digital Design (ECEn 220)

Duties: grading

Enrollment: ~120

Missionary

Fall 2016–Summer 2018

The Church of Jesus Christ of Latter-day Saints

Duties: teaching, training and organizing team of 16

EXPERIENCE

Graduate Researcher

Aug 2022–Present

Brigham Young University

Provo, UT

- Generated synthetic datasets of up to 5,000 circuits (44 GB) for training and evaluation
- Rearchitected FPGA CAD orchestration system for parallel execution and maintainability
- Replaced netlist reverse engineering program, decreasing runtime by 338× and increasing F1 score by 2×
- Developed graph neural network models for FPGA IP identification, improving F1 score by 30–80% while reducing runtime from linear in the number of IP cores to linear per netlist
- Designed and implemented hierarchical Bayesian model to analyze the performance of GNNs with respect to graph structure
- Developed open format for extracting netlists from proprietary tools
- Developed hash-based IP recognition algorithm in Standard ML
- Developed tool to visualize and characterize performance of hash algorithms for hash-based IP recognition

Undergraduate Researcher

Jan 2021–Apr 2022

Brigham Young University

Provo, UT

- Developed a declarative framework for generating FPGA bitstream edge cases, increasing fuzzing coverage for an open-source FPGA toolchain
- Constructed FPGA trojan horses to characterize trojan detection algorithm

PROJECTS

Forth Virtual Machine (C)

- Designed port-mapped stack-based virtual machine with extensible peripheral support
- Implemented associated assembler and compiler

QFM Orthodox File Manager (C)

- Designed lightweight tool to connect pairs of shells with a visual file display

Guac Incremental Computation Library (Standard ML)

- Designed a library supporting incremental updates through computations

Shapes (Standard ML)

- Designed a shape-functor fold/unfold/map library based on Charity

TECHNICAL SKILLS

C, Standard ML, Python, TCL, System Verilog, Vivado, Unix, Git, PyG

SERVICE

Treasurer

Winter 2021–Fall 2022

BYU IEEE Student Branch